DSP Power Consumption and Capacity Projections for WDM-OFDMA-PON

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Abstract: *Wavelength Division Multiplexing- Orthogonal Frequency Division Multiple Access-based Passive Optical Network (WDM-OFDMA-PON) is accepted as one of the most suitable architectures to tackle the requirements for Next Generation Optical Access Networks (NG-OAN). Digital Signal Processing (DSP) is the key technology for the development of this architecture. However, current DSP devices' processing capacity is at least one order of magnitude bellow the required for the implementation of WDM-OFDMA-PON. Additionally, due to the access network's massiveness, the DSP's energy consumption has become a major concern. In order to describe how long it will take for the DSP's devices to cope the requirements for WDM-OFDMA-PON, and how much energy they will consume, in this paper the projections of DSP's capacity and energy consumption were developed, considering different rates of annual improvement of the technology. Based on our projections, we have demonstrated that the required capacity will be achieved within two to five years from now, and such device will consume approximately twice the amount of power of current processors if the annual rates of improvement of capacity and energy efficiency are maintained.*

Keywords: DSP, Next Generation Optical Access Networks, WDM-OFDMA-PON, energy efficiency, power consumption, processing capacity.

1. Introduction

Digital Signal Processing (DSP) is the key technology for the implementation of Next Generation Optical Access Networks (NG-OAN) [1], more specifically for Wavelength Division Multiplexing- Orthogonal Frequency Division Multiple Access- Passive Optical Network (WDM-OFDMA-PON) scheme [2]. This architecture is based on the generation of OFDM in which the data is carried over many lower rate subcarriers. A fundamental challenge to tackle for the implementation of OFDM is the need of a large number of subcarriers. It has been demonstrated that the OFDM modulation/demodulation can be achieved through the Inverse Discrete Fourier Transform (IDFT/DFT) [3-4]. As a consequence, this modulation requires DSP. Optimized algorithms had been developed to compute the DFT, such as the Fast Fourier Transform (FFT), that require a considerably reduced computation compared with DFT. However, even with the implementation of fast algorithms, the needed capacity for computing the FFT for a WDM-OFDMA-PON architecture is at least one order of magnitude higher than the processing capacity of current commercialized DSP [2]. Consequently, the main concern for massively deploying WDM-OFDMA-PON is whether DSP will keep up with the requirements in capacity and energy efficiency of NG-OAN.

WDM-OFDMA-PON is considered as a NG-OAN architecture, since it fulfills most of the requirements of the networks of the future. Among these are; spectral efficiency, high transmission speeds, energy efficiency, and DSP-based transceivers [1].

For the required bandwidth and capacity, Cisco's 2011-2016 forecast project indicates that the overall IP traffic will grow at a compound annual growth rate of 29% from 2011 to 2016. It also points out that more than half of the global internet traffic will be video related. Additionally, it is expected that average broadband speed will experience a 3,8-fold growth [5].

Within the goal of satisfying the ever rising bandwidth demands of end users, energy consumption is no longer a consequence. Rather energy efficiency has become a stringent requirement [6]. It has been estimated that in 2007 ICT produced up to 1%–2% of the worldwide carbon foot-print, and that network infrastructure made up to 25% of that contribution [6-8]. It is expected that in the next decade such energy consumption will grow 2-fold if there are no improvements in energy efficiency [9]. Based on exponential growth trending criteria, network equipment could lead to a unsustainable energy consumption in the next decade [10]. Hence the importance of improving energy efficiency of NG-OAN for reducing its overall power consumption.

DSPs processing capacity depends on the scalability of the number of transistors in a chip and the clock speed [3]. Moore's law indicates that the amount of transistors doubles approximately every eighteen months. Meanwhile Gene's Law indicates that the amount of energy required to execute one million of instructions per second (MIPS) in a DSP is halved every two years [11-12]. In this paper, using the trends in growth of capacity and Gene´s Law, we develop projections of energy consumption and processing capacity for DSP. We determine the time required to cope with requirements and determine whether or not DSP-based WDM-OFDMA-PON transceivers are feasible. Section II presents the requirements for NG-OAN. Section III describes the main components in a WDM-OFDMA-PON architecture. In section IV we explain the considerations used to develop the projections. Section V contains the results with explanatory graphics and discussion. Finally some conclusions are presented in section VI.

2. Requirements for NG-OAN

NG-OANs are expected to fulfill a large list of challenging requirements of the ever increasing demand of Internet services. The foremost requirements are that NG-OAN should support a major number of users, deliver a higher data rate, and lower down energy consumption [1].

NG-OAN should be composed of a multilayer network, through node consolidation, compatible with Gbit/s access rates. Additionally, NG-OAN must offer high scalability and flexibility, guaranteeing end to end performance and survivability. It also needs to assure energy efficiency, and should keep low costs of ownership. Node consolidation is possible by increasing the reach and the number of users supported by the access network [13-14]. Future networks should increase the functionality of the optical domain, in order to take advantage of photonics' scalability, as the traffic volume and bit rates increase [15].

There exist three approaches to achieve OAN's capacity growth: increase the number of wavelengths supported by the fibber, increase the bit rate of every wavelength (spectral efficiency), and reduce the amount of signal distortion accumulated per unit distance [1, 16]. Architectures such as WDM-PON and WDM-OFDM-PON have been widely accepted as possible solutions to fulfill these requirements.

NG-OAN will continue with the trend that enables the technologies of 100 Gbit/s to manage the required capacity. DSP is playing an important role in the transmitter and receiver ends of optical networks, where advanced algorithms can be used to compensate fiber impairments. The nonlinear distortions effects in the optical fiber could be compensated using the high processing capacity of DSPs [1]. Since Moore's law is expected to be valid for sixteen years [3], an important question is to know when the development of high capacity processors will be possible.

Another challenge to tackle for high capacity DSP's implementation in optical networks is energy consumption, since energy efficiency has become an increasingly important aspect for network design. Based on Moore's scaling, a smaller chip would consume less energy, however if the device remains active for a long time it could consume more energy than a larger chip [11]. Multi-core DSP have gained importance due to the high speed processing required, and because of reduced energy consumption and production costs [17].

Is important for NG-OAN to reduce energy consumption and increase energy efficiency. Currently, it is estimated that the Internet uses up about 0,4% of the total energy consumption in broadband-enabled countries, and that it uses ten thousand times more energy than the minimum required [9]. PON is considered as a green technology [18] because of its low power consumption. A solution path in energy consumption in short term will be 10G PON. Nevertheless, for the long term WDM-PON is the technology that has the lowest power consumption. OFDM-PON has the highest power consumption as a result of the implementation of high speed DSP, compared to the aforementioned architectures [19].

3. WDM-OFDMA-PON

Hybrid solutions based on WDM technologies offer a feasible solution to develop terabit capable optical access networks, subject to NG-OAN requirements [1]. Several architectures have been proposed to fulfill these requirements. However, based on its high capacity, scalability, spectral efficiency, data rate and number of users, WDM-OFDMA-PON seems to be the most suitable for NG-OAN [1].

Figure 1 shows the basics of WDM-OFDMA-PON architecture. It consists of generating OFDM subcarriers at the Optical Line Terminal (OLT), and optically modulating them by a set of continuous waves (CW) each at a specific wavelength. All the wavelengths are multiplexed with an Arrayed Waveguide Grating (AWG), and transmitted through a Singular Single Mode Fiber (SSMF). After a few miles, a Local Exchange (LE) amplifies and routes the signals towards the Optical Network Units (ONU). Once the signals reach the ONUs, each one is tuned to a specific wavelength and OFDM subcarrier. For the upstream (US), the OFDM subcarrier is mapped and transmitted in the US wavelength. All the wavelengths are combined and amplified at the LE. The signals are then received coherently by the OLT. This architecture supports λ x N ONUs without compensation for Chromatic Dispersion (CD) [20]. The main obstacles for the implementation of this scheme are the requirements of advanced DSP in the transceivers, high speed Analog to Digital-Digital to Analog converters (ADC/DAC) to achieve the sampling rates needed, and fast Radio Frequency (RF) components to generate the OFDM signals [2].

In spite of the limitations of DSP, Terabit Optical Access Networks Based on WDM-OFDMA-PON have been demonstrated [20-22]. Such demonstration was possible because of the recent development of broad-band, power efficient ADC/DAC chips [20].

3.1 Optical line terminal

The Optical Line Terminal transmits the information through a set of different wavelengths *W*. These wavelengths are intensity modulated by an OFDM multiband signal. Each OFDM sub band is composed of 64^{+} frequency subcarriers, with 16-QAM modulation [20].

The generation of 4^{+} multiband OFDM signals requires high speed and advanced DSPs. It must be able to generate 40^{+} Gbit/s data rate. Multiband OFDM total bandwidth is less than 20 GHz because of the use of multilevel modulation M-QAM. Therefore, it allows the use of commercial ADC/DAC for signal transmission [20, 23-24].

radix-2 algorithm requires the computation of $N/2\ log_2(N)$ butterflies. Since the system is composed of four sub-bands the total number of butterflies is $2N log_2(N)$. For a 48 Gbit/s access rate, the symbol period is T_s = 21.33 ns and a total of 4096 butterflies per symbol are required. For real time processing, the 256 point FFT must be accomplished over a symbol period.

To achieve this, a minimum of 1.92×10^{11} butterflies per second are required. Since each butterfly requires two complex sums and one complex multiplication, assuming four-multiply two-add scheme for each complex multiplication, and two real adds for each complex sum, a minimum of six Multiply Accumulate Operations (MAC) and two memory fetches are needed [26]. The required processing capacity for a DSP should be around 1152 Billions of MACs (GMAC), considering only the MACs operations.

The projections of these parameters are required to determine the time that will take to achieve the processing capacity and energy consumption requirements for DSP's in WDM-OFDMA-PON. It is possible to establish with this information whether the architecture is feasible. Baliga made a projection of Internet's energy consumption including estimations of future efficiency gains [8]. Using an exponential model of efficiency improvement, if a state-of-the-art router or switch has a capacity C_0 and a power consumption P_0, then in t years a state of the art router or switch will have a capacity C_R and a power consumption P_R given by:

$$\frac{P_R}{C_R} = \frac{P_0}{C_0}(1-\alpha)^t \quad (1)$$

where α is the state-of-the-art technology's annual rate of improvement [8]. This type of analysis could be extended to determine the power consumption and capacity trends of DSPs. Separating equation (1) into equations (2) and (3) below, and choosing the appropriate values of annual rate of improvement α, we have:

$$C_R = C_0(1+\beta)^t \quad (2)$$

$$P_R = P_0(1+\gamma)^t \quad (3)$$

where β is defined as the annual rate of improvement in the processing capacity for state-of-the-art DSP, and γ is the annual rate of increase in energy consumption.

Based on the data of energy efficiency improvement and processing capacity according to Gene's work, it can be concluded that the state-of-the-art power efficiency is approximately improving at a rate of 34% per year, i.e., $\alpha \approx 0.3$.

From the capacity point of view, since more devices can be placed into a chip according to Moore's Law, and the clock speed is constantly accelerating, the processing capacity is increasing at a rate of 71% per year, i.e., $\beta \approx$ 0,7 [3]. Comparing the equations (2) and (3) with the equation 1, it can be seen that γ is associated with α and β by the equation 4. According with current data of α and β, the annual rate of power consumption increase is of 19%, i.e., $\gamma \approx 0.19$. In order to extend the analysis, a different set of values for α, β and γ will be considered.

$$\gamma = \beta - \alpha\beta - \alpha \quad (4)$$

Current commercial DSPs, such as the Tilera's Tile64 processor, work at a data rate of 866 MHz with 64 cores (it has been proved with 15 baseband OFDM channels), with a capacity of 443 Billion Operations per Second (BOPS) and an energy consumption of 15 to 22 W, with all cores running at 700 MHz [17, 27]. Texas Instruments' TMS320C6678 Fixed-Point and floating point Digital Signal Processor works at a data rate of 1.25 GHz with eight cores, for a peak capacity of 320000 MMAC, with an estimated power consumption of 13 W, for an average utilization of 50 percent [28]. Fujitsu has been investigating the development of a 100 GHz DSP that has a power consumption of 50 W [23].

5. Results

This section presents processing capacity and power consumption projections for DSP until the year 2030. The aim is to determine the time when the required processing capacity will be available and its feasibility for DSP in WDM-OFDMA-PON. These projections are based on the equations and coefficients provided in the former section and using as reference the Texas Instruments' TMS320C6678 DSP.

DSP chip energy consumption will mainly depend on the potential capacity of those devices. According to Fig. 2, using value of $\beta \approx 0.7$ mentioned in the preceding section, the required capacity to process a 48 Gbit/s per optical channel WDM-OFDMA-PON signal could be achieved within the next two to three years. However, with a slower improvement rate, *e.g.* $\beta \approx 0.3$ it could take more than five years to get to the required DSP's capacity.

The projections for DSP chip's total power consumption capable of processing an OFDM-PON signal depend on the annual improvement of both, the capacity, and the power efficiency. Figure 3 shows the total power consumption of ultra high processing DSP chips assuming the best case scenario for capacity growth (β = 0.7) and different evaluated cases of energy efficiency improvement. According to Fig. 3, for a value of γ = 0.53 in 2016, in which the required capacity is achieved, the device would consume almost 50 W. In the case of γ = 0.19 (which corresponds to current values of α = 0.3 and β = 0.7), future commercialized DSPs with high capacity will consume approximately twice the amount of energy than current commercialized DSPs. In the best case, with α = 0.5 for γ = -0.15, the slope of the curve is negative. This means that in 2016 the same chip will consume almost 8W, 38.5% less than the evaluated DSP.

Considering the projection that in the year 2016 the DSP will have the required capacity for WDM-OFDMA-PON, it is possible to evaluate the case in which the capacity remains constant (assuming β = 0) while the power

efficiency improves with time. For this scenario $\gamma = -\alpha$ and the power consumption of the device will only diminish in time. As shown in Fig. 4, if the value of α =

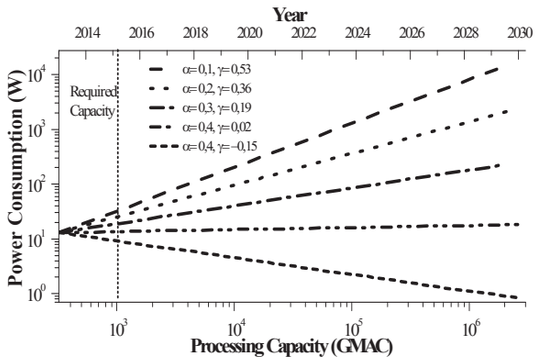

Figure. 3. Power consumption for DSP as a function of the processing capacity for diferent values of α. β is fixed in 0.07.

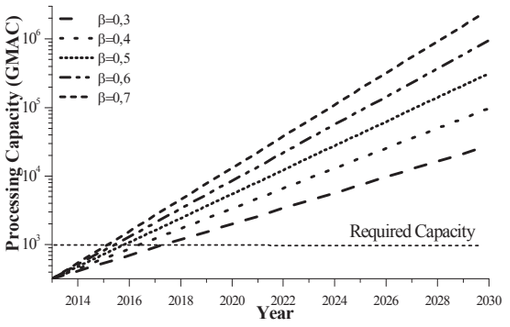

Figure. 2. Projections of the processing capacity increase until the year 2030. It can be noticed that the required capacity will be achieved within the next three to five years.

0.3 is maintained, a DSP capable of processing 1150 GMAC will consume 890 mW in the year 2025. This represents an energy consumption reduction of 93.15%. Considering the different values of α, the power will span from 8.5 W to 45 mW in the year 2025.

According to these results, it seems possible to achieve an ultra high capacity DSP, capable of processing WDM-OFDMA-PON signals. The time needed to achieve such technology could be from two to five years (2015-2018). However, the main constraint for the implementation of DSP-based NG-OAN remains power consumption. In the worst case scenario the power consumption could achieve the alarming figure of 50 W per chip, hence making the implementation of NG-OAN based on WDM-OFDMA-PON not feasible. A possible option is to wait longer time until technology is able to increase energy efficiency, and to decrease overall power consumption. In such case, it could be possible to achieve a 1.3 W DSP chip in the year 2020 or a 45 mW DSP chip in the year 2025 capable of processing 1150 GMAC (assuming $\alpha = 0.3$).

A DSP chip launched in 2006 was studied for validating the projections presented in this work: Texas Instruments' TMS320TCI6482 Fixed-Point Digital Signal Processor, which works at a data rate of 1 GHz with one core DSP. The chip has a capacity of 9.600 MMAC, and an

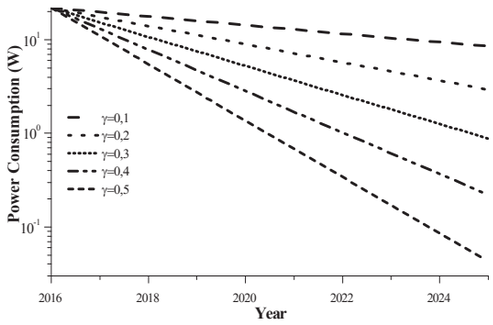

Figure. 4. Power consumption trends of a DSP chip with a fixed capacity of 5.7×10^5 MIPS. Since C is fixed $\gamma=\alpha$.

estimated power consumption of 3.1 W, for an average utilization of 50 percent. Using the proposed capacity and power consumption equations (2) and (3) for the year 2013, the estimated capacity for a DSP would be 393 GMAC and the estimated power consumption 11 W. The validity of the results is demonstrated by comparing these characteristics to the TMS320C6678 DSP chip.

6. Conclusions and future work

We have demonstrated that the required DSP's capacity for NG-OAN will be achieved within two to five years from now; however, such device will consume approximately twice the amount of power of current processors if the annual rates of improvement are maintained. A substantial's annual rate of improvement energy efficiency is required for WDM-OFDMA-PON architectures to massively utilize DSPs as expected. Otherwise, the energy consumption of these advanced chips will not be sustainable, and as a consequence the implementation of high capacity DSP-based NG-OAN will not be feasible. From the capacity point of view, current trends are enough to achieve the required amount of DSP's processing capacity. Based on our results, if current improvement trend of energy efficiency is increased, we should expect that ultra high capacity processors will be massively commercialized within the next two to five years. As such DSPs will consume less or equal power than current commercialized DSPs, the implementation of NG-OAN based on WDM-OFDMA-PON architectures will become possible. The presented projections expose the fact that energy savings methods are of increasing importance in the design of DSP- based NG-OAN.

In future work an analysis of power consumption and bandwidth for Analog to Digital Converters will be realized, since these devices are also limiting for the implementation for OFDM based NG-OAN. With the estimations of power consumption for both ADC and DSPs, the total power consumption for a WDM-OFDMA-PON network will be estimated and compared with existing architectures as PON and WDM-PON. With

these work the feasibility of WDM-OFDMA-PON architectures will be determined.

7. Acknowledgment

The authors want to thank Prometeo Project of SENESCYT (Ecuador) and Universidad de las Fuerzas Armadas (ESPE) extension Latacunga for the financial support to this research work.

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